LOW-POWER DESIGN OF DIGITAL SIGNAL PROCESSING BLOCK FOR INTEGRATED POWER METER

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Abstract *– The paper considers the architecture and low power design aspects of the digital signal processing block (DSP) embedded into a three-phase integrated power meter IC. Power optimization levels are discussed first, and then the arhitecture of the signal-processing block is described together with power-optimization results.*

1. INTRODUCTION

Modern power meter devices relays on single chip referred to as integrated power meter (IPM) [1]. The designed IPM incorporates all the required functional blocks for 3-phase metering, including a precision energy measurement front-end consisting of Sigma Delta AD converters, digital filters and digital signal processing block; 8051 microcontroller, real-time clock, LCD driver and programmable multi-purpose inputs/outputs. The IC requires a minimum of external components, inherently improving meter reliability, simplifying manufacturing process and providing a fast time-to-market metering solution.

The digital signal processing block (DSP) is part of the proposed IPM [2, 3] which performs the precision computations necessary to measure power-line signal parameters: root mean square values for current and voltage, active, reactive and apparent power, active, reactive and apparent energy, signal frequency, power factor, etc.

This paper considers the low power design aspects of DSP embedded into the three-phase integrated power meter IC.

This paper is organized in five sections and References. The following section gives an overview of power optimizations methods. The third section considers the architecture of DSP block. The subsequent section gives gating techniques applied to DSP architecture. The fifth section describes operand isolation technique.

2. POWER CONSUMPTION AND POWER OPTIMIZATION LEVELS

Power consumption in digital circuits has static and dynamic consumption aspects. Static consumption is mainly due to leakage currents. Dynamic power consumption exists due to switching activities and consists of internal power and net power. Internal power dissipation includes switching of the transistors inside the cells and the power dissipated when charging or discharging internal cell net capacitances. Net power is consumed by charging and discharging the chip wires capacitance. For any digital CMOS circuit the dynamic power is given by (1):

$$P_D = A_F \cdot f_{CLK} \cdot C_L \cdot V_{DD}^2 \qquad (1)$$

where A_F is the switching activity factor, C_L the total node capacitances of the circuit and V_{DD} the power supply voltage, [4]. Lowering the dynamic consumption implies reducing some of these factors and can be applied at several levels of abstraction: technology, circuit, gate, architecture and system levels.

Technology level involves fabrication process and considers devices. Optimizations are for instance the use of several threshold V_{TH} and power supply V_{DD} scaling. Mainly consist of using different standard cell libraries with different voltage thresholds (typically low V_{TH} and high V_{TH}) in order to reduce leakage power consumption.

Circuit level is related to gates or cells design. Optimizations may imply the use of power optimized cells.

At the **gate level**, some optimizations are gating and power down techniques. Gated clock is used to reduce switching activity of latches and flip-flops. Entire execution units are stopped by gates when they are not performing useful operations. This is an important concern since units can be switching and consuming power even when they are not being actively utilized. Data gating is used to decrease unwanted switching in combinational logic blocks. The power down reduces static and dynamic consumption, as well.

At the **architectural** level, it is possible to optimize the memory hierarchy or the data-path by retiming or scheduling. The main goal is to reduce dynamic power consumption by reducing activity and wires capacitance. A carefully redesign of the micro-architecture was done to minimize complexity as much as possible.

Finally, at the **system level**, possible techniques are idle modes, voltage selection and power down management. It is possible to use in the same design different voltage islands that can be switched on/off individually or supplied with different voltages.

3. THE ARCHITECTURE OF DSP BLOCK

DSP block accepts 16–bit wide inputs representing voltage, current and phase-shifted voltage samples from digital filters. Thereafter it calculates already mentioned final power line parameters. Three sets of power line measurement results are obtained for different power line phases called R, S and T. The current input dynamic range is from 10 mA RMS to 100 A RMS, while for voltage input it is up to 300V RMS. Results are represented within DSP by 24-bit 2's complement values.

DSP utilizes controller/datapath architecture which consis-

ts of several blocks: finite state machines, three static single port 64x24 bit Random Access Memories, datapath registers, arithmetical units for addition, subtraction, division, square-rooting, multiplication and other digital blocks. Digital blocks can be divided into five main groups (Fig. 1):

1. Frequency measurement circuit
2. RAM memory block
3. Part for I^2, V^2, P, Q accumulating and energy calculation
4. Part for current and voltage RMS, active, reactive and apparent power and power factor calculation);
5. Control unit that manages all other parts of DSP.

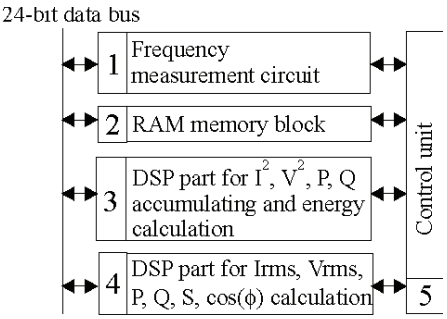

Figure 1. *DSP block diagram(NA SLIC)*

There is a single 24-bit data bus connecting these sub-blocks of DSP. The control path of DSP unit is implemented as a finite state machine and it generates a number of control signals that determine what component can write to 24-bit data, what registers are loaded from the bus and what arithmetical operation is performed. Controller performs the periodically repeated sequence that lasts exactly 1024 clock periods which is divided into four 256 clock period subsequences. The first three FSM subsequences are called R, S and T and they control the calculations made for each phase of the three-phase energy system. During R, S and T subsequences intensive calculations are performed only within subpart 3 (Fig.1). One of the operations in R, S and T subsequences is current square accumulation necessary for obtaining current root-mean-square current value *I*rms.

New result for root-mean-square current, Irms, is calculated once per second according to the expression:

$$Irms = \sqrt{\frac{1}{N}\sum_{n=1}^{N} i(nT)^2} \qquad (2)$$

where the value of constant is N=4096. Current-square $i^2(nT)$ in equation (2) is accumulated over one second period. Thereafter, the sum is divided by N, and root-mean-square current is calculated.

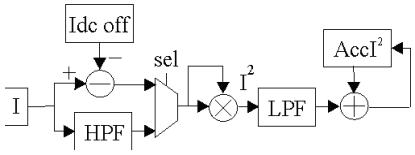

Figure 2. *Data processing chain for current-square accumulation*

The operation sequence for current square accumulating performed by Block 3 in Fig. 1 is given in Fig.2.

The sequence is performed 4096 times per second.

At the beginning of each subsequence R, DC offset has to be removed from instantaneous current values. Two options for DC removal are implemented. First option is to subtract the constant offset determined during calibration procedure. The second is by using the first order digital high pass filter cut-off frequency of 5Hz. HPF transfer function

$$H(z) = \frac{I_{\mathrm{HPF}}(z)}{I(z)} = (1-2^{-10})\frac{1-z^{-1}}{1-z^{-1}(1-2^{-9})} \qquad (3)$$

can be transformed in the following equations implemented by DSP's
hardware:

$$R_{\mathrm{HPF}} = R_{\mathrm{HPF}}(1-1/512) + (1024-1)\cdot(I(n)-I(n-1))$$
$$I_{\mathrm{HPF}} = R_{\mathrm{HPF}}/1024 \qquad (4)$$

where R_{HPF} is the register of the filter, $I(n)$ and $I(n\text{-}1)$ *two* consecutive current values and I_{HPF} is the filter's result.

After DC offset elimination, instantaneous sample of current I is squared in multiplier unit (within sub-block 3). Then, the value I^2 is passed through the single pole Low Pass Filter (LPF) with a cut-off frequency of 10Hz, and accumulated into register AccI^2 (Fig. 2).

Low pass filter helps in reducing the calculation error due to the fact that time-interval of 1 second (that is, accumulating time for the value I^2) does not always happened to be integer number of power-line-signal half-periods. LPF's transfer function

$$H(z) = \frac{I^2_{\mathrm{FILTERED}}(z)}{I^2(z)} = \frac{2^{-6}}{1-z^{-1}(1-2^{-6})} \qquad (5)$$

can be transformed to the following equations:

$$R_{\mathrm{LPF}} = I^2(n) + R_{\mathrm{LPF}}(1-1/4096) \qquad (6)$$

$$I^2_{\mathrm{LPF}} = R_{\mathrm{LPF}}/4096 \qquad (7)$$

where R_{LPF} is the current register of the filter and I^2_{LPF} represents the result after filtering.

HPF and LPF are easy for implementation. Part of a DSP hardware that handles all operations from the current-square accumulation data processing chain is shown in Fig. 3. The LPF and HPF use registers RegA and RegB and arithmetical addition and subtraction units. The registers stored in RAM block are: 24-bit instantaneous current samples I(n) and I(n-1), 48-bit R_{HPF} (that produce DC free current signal I_{HPF} according to Eq. (6)), 48-bit R_{LPF} (input to low-pass filtered square current value I^2_{LPF} , calculated according to Eq. (7)), and 48 bit-accumulated sum AccI^2.

The same procedure is performed and the same hardware is used for V^2 accumulating. Active and reactive power accumulation is done through the same procedure. The only difference is in multiplication process: voltage and current samples values are for active power accumulation, and current-sample value is multiplied with phase-shifted voltage-sample for reactive power accumulation.

The fourth subsequence of the controller, denoted *E*, manages the calculations that are periodically repeated every second. Based on accumulated squares of instantaneous current and voltage, and accumulated instantaneous active and reactive power during the last second, calculations are performed in order to generate voltage and current root mean square (RMS) and mean active and reactive power values, apparent power and power factor. All these calculations are performed in Block 4 in Fig. 1.

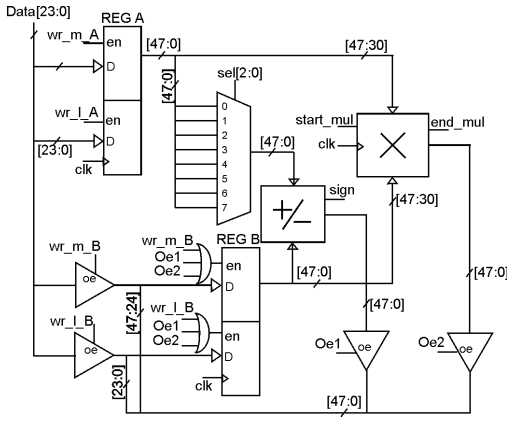

Figure 3 *Structure of Block 3 in Fig. 1*

Power dissipation of DSP block can be broken down into three main areas. The first area is the power cost associated with accesses to the three data memories (Block 2 in the Fig.1). This is made up of the power consumed within the RAM units themselves, and the power required to transmit the data across the large capacitance of the 24-bit data bus. Access to RAM provides the largest part of power consumption in data-dominated applications.

The second main area of power consumption comes from the energy dissipated in performing the actual operations on the data. This is made up of the energy dissipated by transitions within the data path associated with the data, and the control overhead required to perform the operations. The most of dissipated power comes from blocks 3 and 5 and the control unit in Fig. 1. Power reduction of these components will be further elaborated in the next chapters.

Clock power is a major component of signal processing block power consumption because the clock is fed to most of the circuit blocks in the processor and the clock switches every cycle. Considering all clock signals, the clock power is usually a substantial 30-35% of the total DSP power.

4. GATE LEVEL TECHNIQUES APPLIED TO DSP

The utilized standard cell technology AMI CMOS 0.35um, does not allow low power optimizations at technology and circuit level. CMOS transistors have only a single V_{TH} and digital cells operate at 3.3V power supply. Significant power reduction is achieved at gate and architectural level. The DSP clock frequency of 4.194 MHz, is low frequency and represents the one of targets for low-power design.

In the synchronous design style the system clock is connected to the clock pin on every flip-flop in the design. These results in three major components of dynamic power consumption: power consumed by flip flops (this has non zero the internal state to the flip-flops is not changing); power consumed by combinatorial logic whose values are changing on each clock edge; power consumed by the clock buffer tree.

Clock gating is the technique for dynamic power reduction. Usually not all circuits in design are used all the time. This gives rise to power reduction opportunity. By AND-ing the clock with the gate control signal, clock gating disables the clock to a circuit whenever the circuit is not used, avoiding the unnecessary charging and discharging of the capacitors in unused circuits.

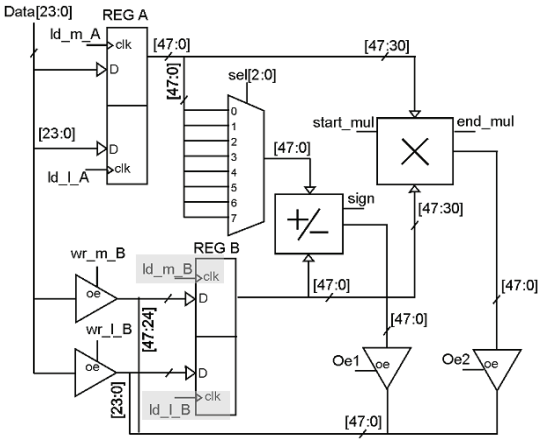

Figure 4 *Block 3 (Fig. 1) optimized for low-power by gating*

The datapath of DSP incorporates arithmetical units for multiplying, dividing and square rooting which are realized as sequential circuits which clock tree is gated. When arithmetical units are unused the clock signal is disabled.

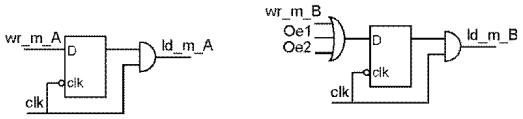

Figure 5 *Clock gating for register writing*

The multiplication unit (Fig.4) input clock signal is gated by subcircuits presented in Fig. 5. Furthermore, the gating of signals is only way to write data into registers and memory block. The clock signals for registers in Block 3 from Fig. 1 are gated also (as shown in Fig.4). The 2 input AND cells with D latch is used as a gate. Figure 5 shows the principle of the gating. The latch based clock gating style adds level sensitive latch to hold the enable signal from the active edge of the clock until the inactive edge of the clock. Since the latch captures the state of the enable signal and holds it until the complete pulse has been generated, the enable signal needs to be stable around the rising edge of the clock.

5. OPERAND ISOLATION TECHNIQUES

Operand isolation techniques are often used to reduce power consumption by selectively blocking the propagation of unused switching activity through the combinatorial circuits.

The multiplexer circuit in Fig.4 incorporates multiple parallel data paths that result in redundant switching activity. To reduce power consumption, three-state buffers are used instead the multiplexer. The modified circuit is shown in Fig.6. The 3-8 decoder circuit (shadowed gray in Fig. 6) provides individual enable signals for the three state buffers (shadowed gray in Fig. 6). A transparent latch is placed behind the decoder

and it is clocked only if its select-output is to change, thus minimizing the switching.

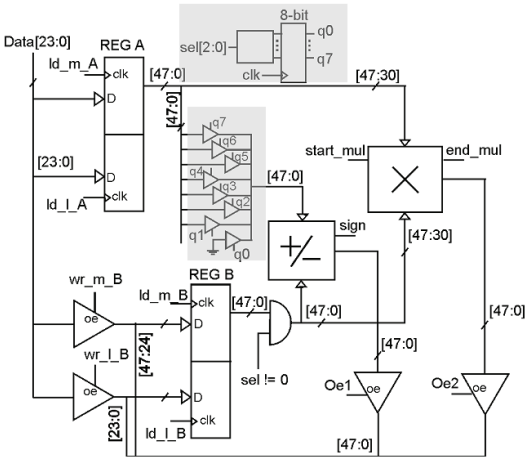

Figure 6 *Block 3 (Fig. 1) optimized for low-power by operand isolation and gating*

The outputs of three state buffers and register B are connected to the inputs of arithmetic circuit for addition or subtraction ("+/-" in Fig. 6). For control signals *sel(2:0)* (the input of 3-8 decoder) in range "001" - "111", the corresponding output enable signal q1 to q7 is active and new data comes from the three state buffers to one of the inputs of arithmetical operator block. For sel(2:0)="000", the write operation into latch is disabled, and thus, the input of the arithmetical operator is not changed. In order to isolate the second operand of arithmetical circuit, register B output is gated with AND gating cells. For control signal in range "001" to "111", data propagation through AND cells is enabled.

6. POWER OPTIMIZATION RESULTS

Switching activity was recorded during the simulations and power dissipation values for the proposed circuits are obtained. The utilized standard cell technology is AMI CMOS 0.35um. First, HDL designs were synthesized and layout was generated by F*irst Encounter* Cadence layout tool. Thereafter the parasitic capacitances of nets are included from the layout. Verilog netlist of the design was extracted and simulated by NCSim simulator. During HDL simulation, switching activity file was obtained and the power consumption results are obtained by the *First Encounter* taking account the parasitic capacitances from layout and switching activity file.

Table 1

power consumption [μW]	original	gating	gating operand isolation
clock tree	150	115	115
registers	3.56	0.03	0.03
three-state circuits	0.15	0.105	0.105
adder	1.11	1.11	0.4
multiplexer	0.045	0.045	0.025
multiplier	6.89	0.068	0.068
fsm circuit	0.889	0.889	0.889
ram memory	150	150	150
total	318.6	267.247	266.517

The obtained power consumption values for circuits from Block 3 in Fig. 1 are given in Table 1. Three power analyses were performed: for original design, gating optimized and operand optimized. Power simulations and technology datasheets showed that most of power consumption is dissipated in clock tree and three pre-built memory blocks SPS4_64x24 supplied by manufacturer. The memories are located near the functional units, to minimize the capacitance of the associated wiring. The memory accesses of $8*10^5$ times gives the power consumption of 150uW. Almost equal power consumption is dissipated by inverters and buffers in the clock tree.

This gating approach gives significant power saving when incorporated into the system reducing the overall power by 17% to 267 μW. The other technique, operand isolation, resulted with minimal power reduction yield.

7. CONCLUSION

This paper considers the low power design aspects of the digital signal processing block (DSP) embedded into three-phase integrated power meter IC. The clock gating technique for dynamic power reduction was successfully implemented into DSP block. By AND-ing the clock with the gate control signal, clock gating disables the clock to a circuit whenever the circuit is not used, avoiding the unnecessary charging and discharging of the unused circuits. On the other hand, the second implemented technique, operand isolation, didn't reduce power consumption significantly.

ACKNOWLEDGEMENT

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Sadržaj – U radu je razmatrana arhitektura i projektovanje DSP bloka (ugrađenog u integrisani merač potrošnje električne energije) sa aspekta minimizovanja njegove snage. Diskutovani su optimizacioni nivoi i opisana arhitektura i rezultrati optimizacije bloka.

PROJEKTOVANJE DSP KOLA ZA SMANJENU POTROŠNJU INTEGRISANOG MERAČA POTROŠNJE ELEKTRIČNE ENERGIJE

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